Claims

- [c1] 1.An electrically erasable and programmable read only memory (EEPROM) cell, comprising:
 - a stacking layer disposed over a substrate, wherein the stacking layer comprises a tunneling dielectric layer, a charge trapping layer and a block dielectric layer sequentially;
 - a gate conductive layer, disposed over the stacking layer; a first source/ drain region and a second source/ drain region, respectively disposed on two sides of the gate conductive layer in the substrate;
 - a first pocket implant doping region, disposed below the stacking layer in the substrate being adjacent to the first source/ drain region; and
 - a second pocket implant doping region, disposed below the stacking layer in the substrate being adjacent to the second source/ drain region, and a doping concentration of the first pocket implant doping region is different from a doping concentration of the second pocket implant doping region.
- [02] 2.The EEPROM cell as recited in claim 1, wherein a dopant type of the first pocket implant doping region and the

second pocket implant doping region is opposite to a dopant type of the first source/ drain region and a second source/ drain region.

- [c3] 3.The EEPROM cell as recited in claim 2, wherein the dopant type of the first pocket implant doping region is P-type.
- [c4] 4. The EEPROM cell as recited in claim 2, wherein the dopant type of the second pocket implant doping region is P-type.
- [05] 5.The EEPROM cell as recited in claim 2, wherein the dopant type of the first source/ drain region is N-type.
- [06] 6.The EEPROM cell as recited in claim 2, wherein the dopant type of the second source/ drain region is N-type.
- [c7] 7.The EEPROM cell as recited in claim 1, wherein a mate-rial of the tunneling dielectric layer comprises silicon oxide.
- [08] 8.The EEPROM cell as recited in claim 1, wherein a material of the charge trapping layer comprises silicon nitride.
- [09] 9.The EEPROM cell as recited in claim 1, wherein a material of the blocking dielectric layer comprises silicon oxide.

[c10] 10.A programming method for an electrically erasable and programmable read only memory (EEPROM) cell, suitable for an EEPROM cell, the EEPROM cell comprising a substrate, a charge trapping layer, a gate conductive layer, a first source/ drain region, a second source/ drain region, a first pocket implant doping region and a second pocket implant doping region, wherein a dopant concentration of the first pocket implant doping region is higher than a dopant concentration of the second pocket implant doping region, the programming method comprising:

applying a bias configuration to the gate conductive layer and the first source/ drain region for performing a first programming, so as to inject electronic charges from the substrate to the charge trapping layer adjacent to the first source/ drain region; and applying the bias configuration to the gate conductive layer and the second source/ drain region for performing a second programming, so as to inject electronic charges from the substrate to the charge trapping layer adjacent to the second source/ drain region, wherein an amount of electronic charges injected during the first programming is larger than an amount of t electronic charges injected during the second programming.

- [c11] 11. The programming method as recited in claim 10, wherein the bias configuration comprises applying 10 volts of voltage to the conductive layer, and applying 5 volts of voltage to the first source/ drain region and the second source/ drain region.
- [c12] 12. The programming method as recited in claim 10, wherein a dopant type of the first pocket implant doping region and the second pocket implant doping region is opposite to a dopant type of the first source/ drain region and the second source/ drain region.
- [c13] 13. The programming method as recited in claim 12, wherein the dopant type of the first pocket implant doping region is P-type.
- [c14] 14. The programming method as recited in claim 12, wherein the dopant type of the second pocket implant doping region is P-type.
- [c15] 15. The programming method as recited in claim 12, wherein the dopant type of the first source/ drain region is N-type.
- [c16] 16. The programming method as recited in claim 12, wherein the dopant type of the second source/ drain region is N-type.

[c17] 17. The programming method as recited in claim 10, wherein a material of the charge trapping layer comprises siliconnitride.